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APPEAL BRIEF TRANSMITTAL		Docket Number: **10191/1614**	Conf. No. **3872**
Application Number **09/720,720**	Filing Date **February 28, 2001**	Examiner **Binh X. TRAN**	Art Unit **1765**
Invention Title **METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING**		Inventor **Richard SPITZ et al.**	

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Date: 9/2, 2003 Reg. No. 36,197

Signature: ______
Jong H. Lee

Further to the Notice of Appeal dated July 25, 2003 (filed at the PTO on July 28, 2003) in the above-referenced application, enclosed are three copies of an Appeal Brief. Accompanying the Appeal Brief is the Appendix to the Appeal Brief.

The Commissioner is hereby authorized to charge payment of the 37 C.F.R. § 1.17(c) appeal brief filing fee of **$320.00,** and any additional fees associated with this communication to the deposit account of **Kenyon & Kenyon**, deposit account number **11-0600**.

Dated: 9/2, 2003

By: ______ (by ______ R. No. 36,197)
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[10191/1614]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants	:	Richard SPITZ et al.
Serial No.	:	09/720,720
Filing Date	:	February 28, 2001
For	:	METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING
Examiner	:	Binh X. TRAN
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Date: 9/2, 2003 Reg. No. 36,197

Signature: [signature]
Jong H. Lee

APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 1.192

SIR:

Applicants filed a Notice of Appeal dated July 25, 2003 (filed at the PTO on July 28, 2003) appealing from the Final Office Action dated March 17, 2003, in which claims 31, 33 and 35 of the above-identified application were finally rejected. This Brief is submitted by Applicants in support of their appeal.

I. REAL PARTY IN INTEREST

The above-identified Applicants and Robert Bosch GmbH of Stuttgart, Germany, are the real parties in interest.

II. RELATED APPEALS AND INTERFERENCES

No appeal or interference which will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal is known to exist to the undersigned attorney or is believed by the undersigned attorney to be known to exist to Applicants.

III. STATUS OF CLAIMS

Claims 16-25 and 27-35 are pending in this application. Claims 16-25, 27-30, 32 and 34 have been allowed. Applicants appealed from the rejection of claims 31, 33 and 35 made in the final Office Action mailed by the Patent Office on March 17, 2003. Of the claims presently on appeal, claim 31 is independent, and claims 33 and 35 ultimately depend from claim 31. The claims on appeal are set forth in the Appendix submitted herewith.

IV. STATUS OF AMENDMENTS

In a Rule 116 Amendment dated June 26, 2003, Applicants amended claims 32 and 34 to be in independent form. The claim amendments to claims 32 and 34 have been entered (according to Examiner's Advisory Action of July 10, 2003).

V. SUMMARY OF THE INVENTION

The present invention relates to a method for eliminating eruptions, impurities, and/or damage in a crystal lattice by selectively etching silicon elements. The method according to the present invention enables etching of silicon elements, in particular surface-plated, sawn-out parts of a silicon wafer, using a gaseous etching medium that selectively etches almost exclusively silicon through a chemical reaction, thus producing gaseous reaction products. (P. 3, l. 6-12). During this selective etching process, surface eruptions, surface impurities, and/or damages in the crystal lattice of the silicon element are eliminated at the same time. (P. 3, l. 12-16). The method according to the present invention further enables stripping damaged silicon zones, in particular of sawn-

out silicon elements, like those that occur, for example, when producing silicon power diodes. (P. 3, l. 16-19).

One advantage of the method according to the present invention is that it is a "batch process," i.e., a process on the wafer level, which means that all sawn-out silicon elements, i.e., chips, of a wafer can be etched simultaneously, which saves a great deal of space and requires only one process step, i.e., handling step. (P. 3, l. 23-29). If necessary, the method according to the present invention can also be used to overetch fully mounted individual diodes, as is currently the case. (P. 3, l. 29-32). A further advantage of the method according to the present invention for selective etching is that it does not use a fluid, thus achieving a clean gas-phase etching of the silicon elements that have been, in particular, sawn out. (P. 3, l. 36 - p. 4, l. 21). Moreover, the method according to the present invention is also less selective toward doping concentrations, resulting in advantageous etched edge profiles and, in particular, prevents a "boron balcony" from forming on the sawn-out and overetched diodes, at the same time increasing mechanical stability and reducing failure rates. (P. 4, l. 2-8).

Another advantage of the present invention is that the selective removal of damaged silicon zones, eruptions or impurities, as well as the planarizing effect of the method according to the present invention. (P. 4, l. 10-13). Due to the high selectivity of the gaseous etching medium used and the chemical reaction that this produces on the surface of the silicon element, and particularly due to the selectivity of this reaction on damage in these zones, it is possible to etch-strip significantly more material, with damaged areas automatically undergoing more aggressive etching, particularly in the edge areas of the sawn-out silicon elements. (P. 4, l. 13-20).

The method according to the present invention for eliminating eruptions, impurities, or damage in the crystal lattice of silicon elements by

selective etching of silicon generally makes use of the characteristic of certain fluorine compounds, known as interhalogens or fluorine-noble gas compounds, to spontaneously etch silicon, i.e., through contact between the fluorine compound and silicon, where this etching action takes place in the gaseous phase, and gaseous reaction products are produced. (P. 6, l. 7-15). To do this, a gaseous silicon-etching fluorine compound, for example, is supplied to a reaction chamber of a reactor that is known per se, in which the silicon elements to be etched were previously placed. (P. 6, l. 15-18). Adsorption of the gas molecules of the gaseous etching medium on the accessible silicon surfaces results in spontaneous, surface-catalytic fragmentation of the etching medium used, thus releasing fluorine radicals that react with the silicon to form a volatile product, e.g., SiF_x (x = 2, 3, 4). (P. 6, l. 18-23). The best known product of a reaction of this type is, for example, stable silicon tetrafluoride SiF_4. (P. 6, l. 23-25). The mechanism can be described as follows, where X is Cl, Br, I or Xe, and n is the number of fluorine atoms in the particular compound:

1. Adsorption: $XF_n \rightarrow XF_n^{adsorb}$

2. Surface-catalytic decomposition: $XF_n^{adsorb} \rightarrow XF_{n-1}^{adsorb} + F^{*,adsorb}$

3. Chemical transformation: $Si + xF^{*,adsorb} \rightarrow SiF_x$ (x = 1, 2, 3, 4)

4. Desorption of reaction products: $SiF_x \rightarrow SiF_x \uparrow$ (x = 2, 3, 4)

in particular: $Si + 4F^{*adsorb} \rightarrow siF_4 \uparrow$

(P. 6, l. 25 - p. 7, l. 3).

Examples of suitable compounds of the XF_n type are the interhalogen compounds chlorine trifluoride, bromine trifluoride and iodine pentafluoride, as well as the noble gas fluoride xenon difluoride. (P. 7, l. 4-7). In the case of the

interhalogen compounds chlorine trifluoride and bromine trifluoride, stripping takes place in a first reaction step of the etching reaction, in which fluorine radicals are released to form stabile chorine fluoride (ClF) and unstable bromine fluoride (BrF), respectively, with two fluorine radicals being generated in each case. (P. 7, l. 26-31). In the case of iodine pentafluoride, the medium is first converted to the relatively stable iodine trifluoride, and in the case of the noble gas fluoride xenon difluoride, elementary xenon is formed in addition to the two fluorine radicals. (P. 7, l. 33 - p. 8, l. 2).

When carrying out the method according to the present invention, one embodiment begins with a silicon wafer from which silicon power diodes are to be produced, with one side of the wafer being doped with an n-type dopant, using an all-over doping step; and the other side being doped with a p-type dopant, using an all-over doping step; a pn-junction thus forms over the entire interior of the silicon wafer. (P. 8, l. 4-11). Afterwards, the wafer that has been pretreated in this manner is provided on both sides with an all-over CrNiVAg plating. (P. 8, l. 12-14).

This silicon wafer is then attached to a commercially available, flexible sawing sheet, made for example from polyvinyl chloride (PVC) or polycarbonate, using an adhesion layer provided on it, and sawn into silicon elements measuring approximately 5 x 5 mm^2 and shaped like squares or hexagons, with the silicon elements being used as silicon power diodes at the end of the manufacturing process. (P. 8, l. 16-23). After the wafer has been sawn, the sawn-out silicon elements produced are first treated in accordance with the present invention while still attached to the sawing sheet, which means that no individual chips are yet produced at this stage, but only an entire unit of sawn-out silicon elements. (P. 8, l. 25-29). It is important to carefully dry the sawn-out silicon elements after sawing the silicon wafer, but before etching, thereby ensuring that no moisture enters the reaction chamber of the reactor used later to carry out the actual selective etching of the silicon elements. (P. 9, l. 6-11).

In doing this, it is advisable to load the sawn-out silicon elements that have been placed on the sawing sheet and are joined to the wafer into the reaction chamber of the reactor using a loading device, such as a load lock, which includes an evacuation and heating function, for example a radiation heater using corresponding lamps. (P. 9, l. 13-18). Pumping out the loading device to create a vacuum and simultaneously heating the wafer that was sawn into silicon elements and is located on the sawing sheet in the loading device, for example using a radiation heater, removes remnants of undesirable moisture particularly efficiently before the wafer that was sawn into silicon elements enters the actual reaction chamber of the reactor, where the described etching reaction takes place after introducing the gaseous etching medium. (P. 9, l. 20-27).

After the sawn silicon wafer, which has been attached to the sawing sheet and dried, enters the reaction chamber of the reactor, the gaseous etching medium is then introduced into this chamber. (P. 10, l. 15-18). When using the interhalogen compounds chlorine trifluoride or bromine trifluoride, the medium is introduced through flow regulators or throttle valves, where the process pressure can range from a low-pressure range, i.e., vacuum, to an atmospheric pressure range. (P. 10, l. 18-22).

After introducing the gaseous etching medium into the reaction chamber, the actual etching of the sawn-out silicon elements begins, where specifically the damaged areas in the crystalline structure, known as damage zones, preferably on the sawn edge are stripped, and the sawn surfaces are planarized. (P. 11, l. 24-29).

The gaseous reaction products produced from the reaction between the gaseous etching medium used and the silicon surfaces are either pumped away continuously, if a throughflow system is used, or accumulated in a reaction chamber that is filled once and then closed, until all gaseous substances are finally pumped out of the reaction chamber upon completion of silicon element

etching. (P. 11, l. 31-37).

The wafer that has been sawn into silicon elements and is attached to the sawing sheet is preferably reheated in the load lock after etching, for example using a radiation heater. (P. 12, l. 17-20). This removes as much leftover etching species as possible before the wafer is removed from the load lock, i.e., leftover gaseous etching medium or leftover gaseous reaction products from the sawn-out, overetched silicon elements or from their surfaces affected by etching. (P. 12, l. 0-24). Leftover media of this type remaining on the surface of the silicon element would result in corrosion when exposed to air, due to the effect of moisture in the air. (P. 12, l. 26-28).

After the processed silicon elements have been discharged from the reactor, they are finally removed individually from the sawing sheet and built up into diodes. (P. 12, l. 30-32).

VI. ISSUES FOR REVIEW

A) Whether claims 31 and 33 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent No. 6,211,010 to Lee et al. ("the Lee reference") in view of U.S. Patent No. 6,077,451 to Takenaka et al. ("the Takenaka reference") and further in view of U.S. Patent No. 6,432,838 to Choi ("the Choi reference").

B) Whether claim 35 is unpatentable under 35 U.S.C. § 103(a) over Lee, Takenaka, Choi in view of U.S. Patent No. 6,136,137 ("Farnworth").

VII. GROUPING OF CLAIMS

For each of ground of rejection discussed in this Brief, all rejected claims do not stand or fall together. For the rejection of claims 31 and 33, the two claims will be argued separately.

VIII. ARGUMENTS

A. § 103(a) Rejection of Claims 31 and 33

Claims 31 and 33 were rejected under 35 U.S.C. § 103(a) as being unpatentable over United over United States Patent No. 6,211,010 to Lee et al. ("the Lee reference") in view of United States Patent No. 6,077,451 to Takenaka et al. ("the Takenaka reference") and further in view of United States Patent No. 6,432,838 to Choi ("the Choi reference"). Applicants respectfully submit that the rejection should be reversed for at least the following reasons.

Claim 31 recites:

> A method for etching, comprising:
> exposing a silicon element to a first heat treatment in a vacuum at a first elevated temperature;
> selectively etching the silicon element with a gaseous etching medium and forming gaseous reactive products, wherein the gaseous etching medium comprises chlorine trifluoride; and
> exposing, subsequent to the selective etching, the silicon element to a second heat treatment in a vacuum at a second elevated temperature.

To establish a prima facie case of obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424F.2d 1382, 1385, 165 U.S.P.Q.

494, 496 (C.C.P.A. 1970). Furthermore, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. See W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984); see also, Akzo N.V. v. United States Int'l Trade Comm'n, 1 U.S.P.Q.2d 1241, 1246 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987)(it is impermissible to pick and choose among individual parts of assorted prior art references as a mosaic to recreate a facsimile of the claimed invention).

In addition to the above, generalized assertions that it would have been obvious to modify the reference teachings do not properly support a § 103 rejection. See In re Fine, supra; In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992). As noted by the Court in the case of In re Fine, "a *prima facie* case of obviousness . . . [can be established] only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 5 U.S.P.Q.2d at 1598 to 1600.

Contrary to the assertions made by the Examiner, the Lee reference does not disclose "exposing, ***subsequent to the selective etching, the silicon element to a heat treatment in a vacuum*** at an elevated temperature," as recited in claim 31. The Examiner contends in the Advisory Action of July 10, 2003, that Figure 5 "shows that after the step of Pre-cleaning, the pressure in the chamber is significantly ***reduced to a flat line after pumping and venting the gas out of the chamber***," and "therefore, [the Examiner] interprets that Lee clearly teaches the step of "exposing, subsequent to the selective etching . . . a second heat treatment in a vacuum at a second elevated temperature." However, Applicants note that the Examiner's interpretation of the "pressure" graph in Fig. 5 leads to illogical results, thereby negating the correctness of the Examiner's interpretation of the Lee reference.

Initially, Applicants note that, in contrast to the Examiner's contention, the pressure line is shown to be at the base of the vertical axis (in the "pressure" graph of Fig. 5) ***at the beginning of the pumping stage*** (after cleaning), and the continues at the base level through the venting stage, all the way until the end of the process. The Examiner's argument is essentially that the literal interpretation of the "pressure" graph in Fig. 5 shows the pressure level falling to the base level of the graph after the "In-situ Pre-cleaning" step, and that this base level of the graph represents vacuum. In this regard, Applicants respectfully point out that the pressure range of 10^{-3} - 10^{-4} Torr for the "In-situ Pre-cleaning" step shown in Fig. 5 is considered a "high" level vacuum. (See, e.g., the following link on the Internet for a definition of various levels of "vacuum":

http://www.mines.edu/fs_home/cwolden/chen435/Lectures/lecture5/tsld002.htm). Given that 10^{-3} - 10^{-4} Torr pressure is considered a "high" level vacuum, the Examiner's literal interpretation of the "pressure [Torr]" graph in Fig. 5 is that most of the steps of the process shown in Fig. 5, including the "start-up," take place at a vacuum level that is significantly higher than a "high" level vacuum, i.e., taking the Examiner's literal interpretation to a logical conclusion, ***<u>at absolute vacuum (0 Torr)</u>***, with the exception of the "Vent" step (rising from 0 Torr to 10^{-3} - 10^{-4} Torr), the "In-situ Pre-cleaning" step (10^{-3} - 10^{-4} Torr), and a portion of the "Pump" step (falling from 10^{-3} - 10^{-4} Torr to 0 Torr). However, this interpretation is clearly illogical, since one of ordinary skill in the art would readily know that an ***<u>absolute vacuum</u>*** is impossible to achieve. This conclusion is further supported by the "Si_2H_6 gas [sccm]" graph in Fig. 5, which clearly shows that "the Si_2H_6 gas is introduced into the chamber during seeding at a flow rate (504) of 15 sccm for 150 seconds" (Lee, column 4, lines 43-44), which means the chamber can't be at an ***<u>absolute vacuum</u>*** as a matter of definition (since Si_2H_6 gas is present in the chamber), which is in turn directly contrary to the Examiner's interpretation of Fig. 5, i.e., that the "Seed Layer" step is performed in ***<u>absolute vacuum</u>***. Furthermore, the Lee reference clearly indicates that "the growth reactor is ***ventilated*** to remove the cleaning gases therefrom." (Col. 3, l.58-59). However, according to the Examiner's interpretation of Fig. 5, the

prevailing pressure is at ***absolute vacuum*** during the "Vent" step, which is simply impossible.

Aside from Fig. 5 of the Lee reference, the only other portion of the Lee reference that deals with process pressure is column 4, lines 3-6: "During in-situ cleaning, the SF_6 and Ar gas mixture is introduced into the chamber of the growth reactor while the pressure (501) of the chamber is maintained to within 10^{-3} - 10^{-4} Torr." There is no mention in the Lee specification of what the process pressure is prior to, or after, the "In-situ Pre-cleaning" step. Applicants respectfully submit that the ramp-up/ramp-down graph lines for the "pressure" quantity shown in Fig. 5 were merely intended to convey the idea of a ***non-zero quantity*** for the pressure characteristic, rather than provide any clear indication regarding what the pressure level is immediately prior to, or after, the "In-situ Pre-cleaning" step. Applicants respectfully submit that a logical interpretation of the overall disclosure of the Lee reference is that a vacuum level of 10^{-3} - 10^{-4} Torr is present in the chamber during the "In-situ Pre-cleaning" step, and this vacuum is ***removed*** after the "In-situ Pre-cleaning" step.

Given the limited disclosure concerning the process pressure in the specification of the Lee reference, it is simply unreasonable to contend that, based on Fig. 5, the Lee reference "clearly teaches the step of 'exposing subsequent to the selective etching . . . a second heat treatment in a vacuum at a second elevated temperature.'" At best, the teaching of Fig. 5 of the Lee reference is ambiguous and contradictory, e.g., the Si_2H_6 gas would have to be introduced into the chamber during the "Seed Layer" step under ***absolute vacuum*** according to the Examiner's interpretation, but this is simply impossible and illogical. Given the limited and ambiguous disclosure of the Lee reference concerning the process pressure, it simply cannot be concluded that a reasonable interpretation of Fig. 5 of the Lee reference clearly indicates that the chamber pressure starts out at ***absolute vacuum*** (at "Start-up"), then transitions to a "high" vacuum level of 10^{-3} - 10^{-4} Torr (in the "In-situ Pre-cleaning" step), then subsequently transitions

back to an absolute vacuum and remains at absolute vacuum for the remainder of the process. A more logical interpretation of the overall disclosure of the Lee reference is that a vacuum level of 10^{-3} - 10^{-4} Torr is present in the chamber during the "In-situ Pre-cleaning" step, and this vacuum is ***removed*** after the "In-situ Pre-cleaning" step.

In contrast to the Examiner's contention, subsequent to the "In-situ Pre-cleaning" step, the disclosure of the Lee reference suggests that the Venting, Seed Layer, and Heat Treatment steps are not performed in a vacuum. While the Examiner relies on step 407 of Figure 4 of the Lee reference for teaching "heat treatment in a vacuum," neither Figure 4 nor the description of step 407 implies that a vacuum is generated prior to the heat treatment. Rather, the process chamber is ventilated prior to step 407, i.e., in step 406: "After the growth reactor is ventilated to remove the cleaning gases therefrom, a seeded layer is formed on the polysilicon (step 406)." (Lee, column 3, lines 58-60).

For at least the foregoing reasons, the Lee reference fails to teach or suggest the step of "exposing, subsequent to the selective etching . . . a second heat treatment in a vacuum at a second elevated temperature."

To the extent the Examiner is asserting that step of "exposing, subsequent to the selective etching . . . a second heat treatment in a vacuum at a second elevated temperature" is an **inherent** characteristic flowing from Fig. 5 and the specification of the Lee reference, Applicants respectfully point out that to rely on inherency, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics *necessarily* flows from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; and see *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Int'f. 1990)). Thus, the M.P.E.P. and the case law make clear that simply because a certain result or characteristic **may** occur in the prior art does not establish the inherency of that result or characteristic.

Clearly, the Examiner has not established that the allegedly inherent characteristics *necessarily* flows from the teachings of the applied art.

In addition to the above, the Takenaka and Choi references simply do not address the step of a heat treatment in a vacuum subsequent to the etching process.

Furthermore, as a noted by the Examiner, the Lee and Takenaka references fail to disclose "exposing a silicon element to a first heat treatment in a vacuum at a first elevated temperature." The Examiner cites a passage from the Choi reference (column 5, lines 25-33) as describing this step. However, this passage merely discloses that the ***etching step is performed in a vacuum***, not the heat treatment. According to the Choi reference:

> It [ClF_3] can be used in the low temperature state as well as plasma state, and has the excellent chemical selectively so that it performs etching at the potions where plasma cannot reach. It also has the advantage that it is highly unlikely to generate particles that could contaminate the wafer surface. In use ClF_3 is generally diluted to a concentration of 20±5 volume % with an inert gas such as N_2. While the lower pressure in the process chamber is good for the uniform etch for the layer inside the chamber, the higher mixing rate of etch gas is good for increasing the etch rate. It is preferable to heat the process chamber to a temperature higher than the boiling point of the ClF_3, prior to the introduction of ClF_3 and preferably higher than 400° C. (Choi, col. 5, ll. 17-30).

Thus, the Choi reference discloses that the heating process is performed prior to the introduction of the ClF_3. ***The Choi reference does not disclose that the heat processing is carried out in a vacuum***. The description of the lower pressure inside the process chamber describes the etching nature of the ClF_3. The ClF_3 is introduced into the chamber after the heating process. While a vacuum is present during the ClF_3 etching process, there is no disclosure that a vacuum is present during any other process including the pre-heating of the chamber. Therefore, the Choi reference does not teach or suggest "exposing a silicon element to a first heat treatment in a vacuum at a first elevated

temperature."

In response to the Applicants' arguments, the Examiner contends the following in the Advisory Action of July 10, 2003:

> Choi teaches the etching step is performed in a vacuum chamber having pump using ClF_3 etchant gas under low pressure. The low pressure exists in the chamber due to the flow of ClF_3 etchant in conjunction with the pump being turned on. Prior to the introduction of ClF_3 (i.e., there is no ClF_3 gas in the chamber), the vacuum must exist because of the pump.

Applicants respectfully note that there is no explicit disclosure in the Choi reference regarding the claimed limitation of "a first heat treatment in a vacuum at a first elevated temperature," as recited in claim 31. The Examiner's argument is essentially that this claimed limitation is inherently taught by the disclosure of Choi. However, in order to rely on inherency, the Examiner must provide a "basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics *necessarily* flows from the teachings of the applied art." (See M.P.E.P. § 2112; emphasis in original; and see *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Int'f. 1990)). Thus, the M.P.E.P. and the case law make clear that simply because a certain result or characteristic **may** occur in the prior art does not establish the inherency of that result or characteristic. While the Examiner contends that "[p]rior to the introduction of ClF_3 (i.e., there is no ClF_3 gas in the chamber), the vacuum must exist because of the pump," it simply does not ***necessarily follow*** that Choi teaches "a silicon element [is exposed] to a first heat treatment in a vacuum at a first elevated temperature," since ***the first heat treatment can certainly take place prior to the introduction of vacuum environment*** in Choi (Choi simply doesn't indicate when the vacuum is introduced relative to the timing of the first heating).

For at least the foregoing reasons, the combination of Lee, Takenaka and Choi fails to render obvious claim 31 and its dependent claim 33.

Independent of the above, claim 33 is separately patentable over the combination of Lee, Takenaka and Choi for the following reasons. Regarding claim 33, neither the Lee nor the Choi reference discloses that the heat treatment is accomplished in a vacuum lock chamber. According to the Lee reference, the only vacuum applied occurs during the etching process in the process chamber, not in a vacuum lock chamber. (*See* Lee, Figure 5.) Also, the Choi reference, as discussed above, only describes a vacuum during the etching process occurring in the process chamber, but not in the vacuum lock chamber. Furthermore, Takenaka simply doesn't teach that the heat treatment is accomplished in a vacuum lock chamber. Therefore, the Lee, Choi and Takenaka references fail to disclose that "at least one of the first and the second heat treatment is accomplished in a vacuum lock chamber," as recited in Claim 33.

For the foregoing reasons, Applicants respectfully submit that the Lee, Takenaka, and Choi references do not render Claims 31 and 33 obvious under 35 U.S.C. §103(a). Reversal of the obviousness rejection of claims 31 and 33 is requested.

B. § 103(a) Rejection of Claim 35

Claim 35, which depends from Claim 31, stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, Takenaka and Choi in view of U.S. Patent No. 6,136,137 to Farnworth ("Farnworth").

To establish a prima facie case of obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re

Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Furthermore, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. See W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984); see also, Akzo N.V. v. United States Int'l Trade Comm'n, 1 U.S.P.Q.2d 1241, 1246 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987)(it is impermissible to pick and choose among individual parts of assorted prior art references as a mosaic to recreate a facsimile of the claimed invention).

In addition to the above, generalized assertions that it would have been obvious to modify the reference teachings do not properly support a § 103 rejection. See In re Fine, supra; In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992). As noted by the Court in the case of In re Fine, "a *prima facie* case of obviousness . . . [can be established] only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 5 U.S.P.Q.2d at 1598 to 1600.

Regarding claim 31, from which claim 35 depends, the Examiner contends in the Advisory Action of July 10, 2003, that Figure 5 of Lee "shows that after the step of Pre-cleaning, the pressure in the chamber is significantly ***reduced to a flat line after pumping and venting the gas out of the chamber***," and "therefore, [the Examiner] interprets that Lee clearly teaches the

step of "exposing, subsequent to the selective etching . . . a second heat treatment in a vacuum at a second elevated temperature." The Examiner's argument is essentially that the literal interpretation of the "pressure" graph in Fig. 5 of Lee shows the pressure level falling to the base level of the graph after the "In-situ Pre-cleaning" step, and that this base level of the graph represents vacuum.

Given that 10^{-3} - 10^{-4} Torr pressure is considered a "high" level vacuum, the Examiner's literal interpretation of the "pressure [Torr]" graph in Fig. 5 is that most of the steps of the process shown in Fig. 5, including the "start-up," take place at a vacuum level that is significantly higher than a "high" level vacuum, i.e., taking the Examiner's literal interpretation to a logical conclusion, ***at absolute vacuum (0 Torr)***, with the exception of the "Vent" step (rising from 0 Torr to 10^{-3} - 10^{-4} Torr), the "In-situ Pre-cleaning" step (10^{-3} - 10^{-4} Torr), and a portion of the "Pump" step (falling from 10^{-3} - 10^{-4} Torr to 0 Torr). However, this interpretation is clearly illogical, since one of ordinary skill in the art would readily know that an ***absolute vacuum*** is impossible to achieve. This conclusion is further supported by the "Si_2H_6 gas [sccm]" graph in Fig. 5, which clearly shows that "the Si_2H_6 gas is introduced into the chamber during seeding at a flow rate (504) of 15 sccm for 150 seconds" (Lee, column 4, lines 43-44), which means the chamber can't be at an ***absolute vacuum*** as a matter of definition (since Si_2H_6 gas is present in the chamber), which is in turn directly contrary to the Examiner's interpretation of Fig. 5, i.e., that the "Seed Layer" step is performed in ***absolute vacuum***. Furthermore, the Lee reference clearly indicates that "the growth reactor is ***ventilated*** to remove the cleaning gases therefrom." (Col. 3, l.58-59). However, according to the Examiner's interpretation of Fig. 5, the prevailing pressure is at ***absolute vacuum*** during the "Vent" step, which is simply impossible.

Applicants respectfully submit that the ramp-up/ramp-down graph lines for the "pressure" quantity shown in Fig. 5 of Lee were merely intended to convey the idea of a ***non-zero quantity*** for the pressure characteristic, rather

than provide any clear indication regarding what the pressure level is immediately prior to, or after, the "In-situ Pre-cleaning" step. Applicants respectfully submit that a logical interpretation of the overall disclosure of the Lee reference is that a vacuum level of 10^{-3} - 10^{-4} Torr is present in the chamber during the "In-situ Pre-cleaning" step, and this vacuum is ***removed*** after the "In-situ Pre-cleaning" step.

For at least the foregoing reasons, the Lee reference fails to teach or suggest the step of "exposing, subsequent to the selective etching . . . a second heat treatment in a vacuum at a second elevated temperature." In addition to the above, the Takenaka and Choi references simply do not address the step of a heat treatment in a vacuum subsequent to the etching process.

Furthermore, as a noted by the Examiner, the Lee and Takenaka references fail to disclose "exposing a silicon element to a first heat treatment in a vacuum at a first elevated temperature." While the Examiner cites a passage from the Choi reference (column 5, lines 25-33) as describing this step, this conclusion is not supported by the cited passage. While the Examiner contends that "[p]rior to the introduction of ClF_3 (i.e., there is no ClF_3 gas in the chamber), the vacuum must exist because of the pump," it simply does not ***necessarily follow*** that Choi teaches "a silicon element [is exposed] to a first heat treatment in a vacuum at a first elevated temperature," since ***the first heat treatment can certainly take place prior to the introduction of vacuum environment*** in Choi (Choi simply doesn't indicate when the vacuum is introduced relative to the timing of the first heating).

For at least the foregoing reasons, the combination of Lee, Takenaka and Choi fails to render obvious claim 31. In addition to the above, Farnworth similarly fails to teach or suggest the above features of claim 31 which are not taught or suggested by Lee, Takenaka and Choi. In fact, the Examiner cited Farnworth solely for teaching "the substrate surface can be a sawn-out part of the

silicon wafer." (3/17/03 Final Office Action, p. 3). Accordingly, claim 35, which depends from claim 31, is allowable over the combination of Lee, Takenaka, Choi and Farnworth.

IX. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the final rejection of claims 31, 33 and 35 should be reversed.

Respectfully submitted,

KENYON & KENYON

Dated: 9/2, 2003

By: ~~Richard L. Mayer~~ (by R. No. 36,197)
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PATENT TRADEMARK OFFICE

[10191/1614]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants	:	Richard SPITZ et al.
Serial No.	:	09/720,720
Filing Date	:	February 28, 2001
For	:	METHOD FOR ELIMINATING DEFECTS IN SILICON ELEMENTS THROUGH SELECTIVE ETCHING
Examiner	:	Binh X. TRAN
Art Unit	:	1765
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Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

Date: 9/2, 2003 Reg. No. 36,197

Signature: [signature]
Jong H. Lee

APPENDIX TO APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 1.192

SIR:

The claims involved in this appeal, claims 31, 33 and 35, in their current form after entry of all amendments presented during the course of prosecution, are set forth below:

APPEALED CLAIMS:

31. A method for etching, comprising:

exposing a silicon element to a first heat treatment in a vacuum at a first elevated temperature;

selectively etching the silicon element with a gaseous etching medium and forming gaseous reactive products, wherein the gaseous etching medium comprises chlorine trifluoride; and

exposing, subsequent to the selective etching, the silicon element to a second heat treatment in a vacuum at a second elevated temperature.

33. The method as recited in Claim 31, wherein at least one of the first and the second heat treatment is accomplished in a vacuum lock chamber.

35. The method as recited in Claim 31, wherein the silicon element is a surface-plated, sawn-out part of a silicon wafer, and at least one of an eruption, impurity and damage in a crystal lattice of the silicon element is eliminated by the selective etching.

Respectfully submitted,

KENYON & KENYON

Dated: 9/2, 2003

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